



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,729	07/30/2004	Cheng Chang Kuo	13135-US-PA	4728
31561	7590	09/23/2005	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			TRINH, HOA B	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/710,729		KUO, CHENG CHANG	
	<b>Examiner</b>		<b>Art Unit</b>	
	Vikki H. Trinh		2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 July 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group I, claims 1-9, in the reply filed on July 14, 2005, is acknowledged.

Claims 10-13 have been canceled. Claims 1-9 are pending in this present application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Han et al. (US 2003/0155572 A1) (hereinafter Han).

As to claim 1, Han discloses a LTPS-TFT structure (page 3, paragraph [0037] ) disposed on a substrate 1 (fig. 5D) comprising a cap layer 3 (fig. 5D) with a gap 10 (fig. 5D) between the cap 3 and the substrate 1; a polysilicon film 4, 4A, 4B (figs. 5B-5D, and paragraphs [0034], [0038], [0039]) disposed over the cap layer 3, wherein the polysilicon film 4B has a channel region 4B and a source/drain region 7, 6 (fig. 5D) on each side of the channel 4B and the channel 4B is directly over the gap 10; and a gate 12 (fig. 5D) disposed above the channel region 4B of the polysilicon film (fig. 5D).

As to claim 2, Han discloses a buffer layer 2 (fig. 5D) positioned between the cap layer and the substrate, so that the gap 10 is positioned between the cap layer 3 and the buffer layer 2 (fig. 5D).

As to claim 3, Han discloses that the gap 10 has a coefficient of thermal conductivity smaller than the coefficient of the thermal conductivity of the buffer layer. Note that the gap is an air gap and the buffer layer is an oxide material (page 2, paragraph [0024]).

As to claim 4, Han discloses that the gap 10 has a coefficient of thermal conductivity smaller than the coefficient of the thermal conductivity of the substrate 1. Note that the gap is an air gap and the substrate is a crystal or glass (page 2, paragraph [0024] and [0030]).

As to claim 5, Han discloses a gate dielectric layer 11 (fig. 5D) disposed over the polysilicon film 4B (fig. 5D).

As to claim 6, Han teaches that the grain size of the channel region 4B (fig. 5D) of the polysilicon layer is on average greater than the grain size of the source/drain region 6, 7 (fig. 5D, and paragraph [0034]).

As to claim 7, Han shows that the width of the gate 12 (fig. 5D) is smaller than the grain size of the channel 4B (fig. 5D).

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2814

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Han, as applied to claim 1 above, in view of Sun et al. (6,936,848) (hereinafter Sun).

Han discloses the invention substantially as claimed, except that the gate is a dual gate structure.

Sun discloses an analogous LTPS-TFT device having a dual gate structure (col. 2, lines 18-20, and col. 3, lines 45-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Han with a dual gate structure, as taught by Sun, so as to prevent current leakage (col. 2, line 19).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Han, as applied to claim 1 above, in view of Peng et al. (6,835,606) (hereinafter Peng).

Han discloses the invention substantially as claimed. Also, Han discloses a dielectric layer (page 3, paragraph [0036] disposed over the polysilicon film 4B (fig. 5D) and the gate 12 (fig. 5D), wherein the dielectric layer (page 3, paragraph [0036] has a plurality of contact windows (contact holes) (page 3, paragraph [0036] ); a passivation layer and a source/drain

Art Unit: 2814

conductive layer (metal connections) (page 3, paragraph [0036]) However, Han does not explicitly teach that the source/ drain conductive layer is electrically connected to the polysilicon film in the source/drain region through the contact window.

Peng discloses an analogous LTPS-TFT device having a S/D regions 210 (figs. 2F, 2G), a channel region 204b of polysilicon film with grains size being larger on average than the S/D regions' grain size, a gate insulating layer 212, a gate 226b over the gate insulating layer, a dielectric layer 228 disposed over the gate, wherein the dielectric layer forms contact windows or holes 230 (fig. 2G) to expose the S/D region, a source/drain conductive layer (metallic layer) 232 (fig. 2G) formed over the dielectric layer 228 to electrically connect the S/D region 210, and a passivation layer 236 disposed over the gate dielectric layer and the source/drain conductive layer 232 (See figs. 2F, 2G).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Han with the source/drain conductive layer formed over the dielectric layer to electrically connect the source/drain region through the contact window, as taught by Peng, so as to provide an electrical connection between the conductive layer and the source/drain region through the opening (col. 5, lines 24-26).

### **Conclusion**

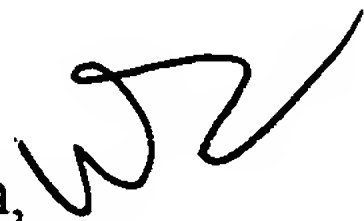
Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If

Art Unit: 2814

attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site ([www.uspto.gov](http://www.uspto.gov)), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh,   
Patent Examiner  
AU 2814